IN THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

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1. (previously presented) A machine-readable medium having stored thereon instructions, which when executed by one or more processors, cause said one or more processors to perform a method, said method comprising:

a) creating a string that models a trace, said string having a collection of lumped elements including cross capacitors;

b) reducing said string to a pi model, said pi model having a pair of cross capacitors; and

c) simulating the application of an applied noise voltage to at least one of said cross capacitors.

2. (previously presented) The machine-readable medium of claim 1 wherein said reducing said string to a pi model further comprises reducing the number of capacitors and resistors in said string.

3. (original) The machine-readable medium of claim 2 wherein said reducing said string to a pi model further comprises reducing six capacitors and two resistors in said string to four capacitors and one resistor.

4. (original) The machine-readable medium of claim 3 wherein said reduction of six resistors and four capacitors is performed according to an Elmore influenced reduction method.

5. (original) The machine-readable medium of claim 3 wherein said reduction of resistors and capacitors is performed according to an O'Brien/Savarino influenced reduction method.

6. (original) The machine-readable medium of claim 1 wherein said string further comprises a number of paths, said reduction of said string to a pi model performed for one of said paths.

7. (original) The machine-readable medium of claim 1 wherein said application of a noise voltage further comprises applying a voltage ramp as said applied noise voltage.

8. (original) The machine-readable medium of claim 7 wherein the ramp time of said voltage ramp is multiplied by a factor to correct for the characteristics of an actual driving transistor.

9. (previously presented) The machine-readable medium of claim 1 wherein said instructions are such that said reducing said string to a pi model may be performed

on a first apparatus and said creating a string that models a trace may be performed on a second apparatus.

10. (previously presented) The machine-readable medium of claim 1 wherein said method further comprises adding a resistor to said pi model as a linear source model.

11. (previously presented) The machine-readable medium of claim 1 said method further comprises allowing a user to observe a noise voltage waveform on a victim node of said pi model.

12. (previously presented) The machine-readable medium of claim 1 wherein said method further comprises calculating the peak noise voltage on a victim node of said pi model caused by said applied noise voltage.

13. (previously presented) The machine-readable medium of claim 1 wherein said method further comprises applying a second applied noise voltage to a second cross capacitor of said cross capacitors.

14. (original) The machine-readable medium of claim 13 wherein said applied noise voltage and said second applied noise voltage are voltage ramps having their end or ramp times in phase.

15. (previously presented) The machine-readable medium of claim 13 wherein said method further comprises calculating the peak noise caused by said applied noise voltage and said second applied noise voltage at a source point of said pi model.

16. (previously presented) The machine-readable medium of claim 13 wherein said method further comprises calculating the peak noise caused by said applied noise voltage and said second applied noise voltage at a load point of said pi model.

17. (currently amended) The machine-readable medium of claim 1 wherein said reducing said string to a pi model further comprises reducing said string to a reduced string then reducing said reduced string to a simple string having resistors ~~is~~ in series and capacitors in parallel, said capacitors separated by one of said resistances, then reducing said simple string to a pi-model.

18. (previously presented) A machine-readable medium having stored thereon instructions, which when executed by one or more processors, cause said one or more processors to perform a method, said method comprising:

a) creating a string that models a trace, said string having a collection of lumped elements, at least one of said lumped elements having a plurality of cross capacitors on a node, each of said cross capacitors corresponding to a different proximate trace;

b) adding said plurality of cross capacitors together to form a reduced string;

c) reducing said reduced string to a pi model, said pi model having a cross capacitor; and

d) simulating the application of an applied noise voltage to said cross capacitor.

19. (previously presented) The machine-readable medium of claim 18 wherein said reducing said reduced string to a pi model further comprises reducing the number of capacitors and resistors in said reduced string.

20. (previously presented) The machine-readable medium of claim 19 wherein said reducing said reduced string to a pi model further comprises reducing six capacitors and two resistors in said string to four capacitors and one resistor.

21. (original) The machine-readable medium of claim 20 wherein said reduction of six resistors and four capacitors is performed according to an Elmore influenced reduction method.

22. (original) The machine-readable medium of claim 20 wherein said reduction of resistors and capacitors is performed according to an O'Brien/Savarino influenced reduction method.

23. (original) The machine-readable medium of claim 18 wherein said string further comprises a number of paths, said reduction of said string to a pi model performed for one of said paths.

24. (previously presented) The machine-readable medium of claim 18 wherein said applying a noise voltage further comprises applying a voltage ramp as said applied noise voltage.

25. (original) The machine-readable medium of claim 24 wherein said voltage ramp further comprises an equivalent ramp time that approximates the worst case noise caused by said plurality of proximate traces.

26. (previously presented) The machine-readable medium of claim 18 wherein said reducing said reduced string to a pi model may be performed on a first apparatus and said creating a string that models a trace may be performed on a second apparatus.

27. (previously presented) The machine-readable medium of claim 18 wherein said reducing said reduced string to a pi model further comprises reducing said reduced string to a simple string then reducing said simple string to a pi-model.

28. (previously presented) An apparatus, comprising:

a computer having design tool software, said design tool software comprised of instructions that when executed cause a method to be performed, said method comprising:

a) recognizing a string that models a trace, said string having a collection of lumped elements including cross capacitors;

b) reducing said string to a pi model, said pi model having a pair of cross capacitors; and

c) simulating the application of an applied noise voltage to at least one of said cross capacitors.

29. (currently amended) A machine-readable medium having stored thereon instructions which when executed by one or more processors cause said one or more processors to perform a method, said method comprising:

calculating a plurality of incremental values from an overall applied noise voltage waveform and simulating the application of each of said plurality of incremental values to a cross capacitor, said cross capacitor one of a pair of cross capacitors associated with a pi model, said pi model reduced from a string having more than a pair of cross capacitors.

30. (previously presented) The machine-readable medium of claim 29 wherein said method further comprises assembling a plurality of observed noise voltages from the simulation of the application of each of said discrete samples.

31. (previously presented) The machine-readable medium of claim 30 wherein said method further comprises displaying an overall observed noise voltage waveform produced from said plurality of observed noise voltages.

32. (original) The machine-readable medium of claim 29 wherein said overall applied noise voltage waveform is a ramp.

33. (previously presented) A method, comprising:

a) creating a string that models a trace, said string having a collection of lumped elements including cross capacitors;

b) reducing said string to a pi model, said pi model having a pair of cross capacitors; and

c) simulating the application of an applied noise voltage to at least one of said cross capacitors.

34. (previously presented) The method of claim 33 wherein said reducing said string to a pi model further comprises reducing the number of capacitors and resistors in said string.

35. (original) The method of claim 34 wherein said reducing said string to a pi model further comprises reducing six capacitors and two resistors in said string to four capacitors and one resistor.

36. (original) The method of claim 35 wherein said reduction of six resistors and four capacitors is performed according to an Elmore influenced reduction method.

37. (original) The method of claim 35 wherein said reduction of resistors and capacitors is performed according to an O'Brien/Savarino influenced reduction method.

38. (original) The method of claim 33 wherein said string further comprises a number of paths, said reduction of said string to a pi model performed for one of said paths.

39. (original) The method of claim 33 wherein said application of a noise voltage further comprises applying a voltage ramp as said applied noise voltage.

40. (original) The method of claim 39 wherein the ramp time of said voltage ramp is multiplied by a factor to correct for the characteristics of an actual driving transistor.

41. (previously presented) The method of claim 33 wherein said reducing said string to a pi model is performed on a first apparatus and said creating a string that models a trace is performed on a second apparatus.

42. (previously presented) The method of claim 33 further comprising adding a resistor to said pi model as a linear source model.

43. (previously presented) The method of claim 33 further comprising observing noise voltage on a victim node of said pi model.

44. (previously presented) The method of claim 33 further comprising calculating the peak noise voltage on a victim node of said pi model caused by said applied noise voltage.

45. (previously presented) The method of claim 33 further comprising applying a second applied noise voltage to a second cross capacitor of cross capacitors.

46. (original) The method of claim 45 wherein said applied noise voltage and said second applied noise voltage are voltage ramps having their end or ramp times in phase.

47. (previously presented) The method of claim 45 further comprising calculating the peak noise caused by said applied noise voltage and said second applied noise voltage at a source point of said pi model.

48. (previously presented) The method of claim 45 further comprising calculating the peak noise caused by said applied noise voltage and said second applied noise voltage at a load point of said pi model.

49. (previously presented) The method of claim 33 wherein said reducing said string to a pi model further comprises reducing said string to a reduced string then reducing said reduced string to a simple string having resistors and capacitors in parallel, said capacitors separated by one of said resistors then reducing said simple string to a pi-model.

50. (previously presented) A method, comprising:

a) creating a string that models a trace, said string having a collection of lumped elements, at least one of said lumped elements having a plurality of cross capacitors on a node, each of said cross capacitors corresponding to a different proximate trace;

b) adding said plurality of cross capacitors together to form a reduced string;

c) reducing said reduced string to a pi model, said pi model having a cross capacitor; and

d) simulating the application of an applied noise voltage to said cross capacitor.

51. (previously presented) The method of claim 50 wherein said reducing said reduced string to a pi model further comprises reducing the number of capacitors and resistors in said reduced string.

52. (previously presented) The method of claim 51 wherein said reducing said reduced string to a pi model further comprises reducing six capacitors and two resistors in said string to four capacitors and one resistor.

53. (original) The method of claim 52 wherein said reduction of six resistors and four capacitors is performed according to an Elmore influenced reduction method.

54. (original) The method of claim 52 wherein said reduction of resistors and capacitors is performed according to an O'Brien/Savarino influenced reduction method.

55. (original) The machine-readable medium of claim 50 wherein said string further comprises a number of paths, said reduction of said string to a pi model performed for one of said paths.

56. (previously presented) The method of claim 50 wherein said applying a noise voltage further comprises applying a voltage ramp as said applied noise voltage.

57. (original) The method of claim 56 wherein said voltage ramp further comprises an equivalent ramp time that approximates the worst case noise caused by said plurality of proximate traces.

58. (previously presented) The method of claim 50 wherein said reducing said reduced string to a pi model is performed on a first apparatus and said creating a string that models a trace is performed on a second apparatus.

59. (previously presented) The method of claim 50 wherein said reducing said reduced string to a pi model further comprises reducing said reduced string to a simple string then reducing said simple string to a pi-model.

60. (currently amended) A method, comprising:

calculating a plurality of incremental values from an overall applied noise voltage waveform and simulating the application of each of said plurality of incremental values to a cross capacitor, said cross capacitor one of a pair of cross capacitors associated with a pi model, said pi model reduced from a string having more than a pair of cross capacitors.

61. (previously presented) The method of claim 60 further comprising assembling a plurality of observed noise voltages from the simulation of the application of each of said incremental values.

62. (previously presented) The method of claim 61 further comprising displaying an overall observed noise voltage waveform produced from said plurality of observed noise voltages.

63. (original) The method of claim 60 wherein said overall applied noise voltage waveform is a ramp.

COMMENTS

The enclosed is responsive to the Examiner's Final Office Action mailed on September 8, 2003 and is being filed pursuant to a Request for Continued Examination (RCE) as provided under 37 CFR 1.114 which has been filed herewith. At the time the Examiner mailed the Final Office Action claims 1 – 63 were pending. By way of the present response the Applicant has: 1) amended claims 17, 29 and 60; and, 2) not added or canceled any claims. As such claims 1 – 63 remain pending. The Applicant respectfully requests re-consideration of the present application and the allowance of claims 1 – 63.

The Examiner has upheld a theory of rejection that each of the Applicant's independent claims 1, 18, 28, 29, 33, 50 and 60 are obvious under 35 USC 103(a) in light of the combination of U.S. Patent No. 6,192,330 (hereinafter, "Nakamura"), U.S. Patent No. 6,314,546 (hereinafter, "Muddu") and U.S. Patent 6,028,989 (hereinafter, "Dansky").

The Applicant's position is that, at least, and for reasons already stated in an Office Action response mailed June 16, 2003 (to which the Examiner is again referred):

1) with respect to independent claims 1, 28, and 33:

the claim limitation "reducing a string to a pi model, the pi model having a pair of cross capacitors" is not taught or suggested by any combination of matter disclosed in Nakamura, Muddu and Dansky;

2) with respect to independent claims 29 and 60:

the claims limitation "a pair of cross capacitors associated with a pi model, the pi model reduced from a string having more than a pair of cross capacitors" is not taught or suggested by any combination of matter disclosed in Nakamura, Muddu and Dansky;

3) with respect to independent claims 18 and 50:

the claim limitation "a plurality of cross capacitors on a node, each of the cross capacitors corresponding to a different proximate trace" is not taught or suggested by any combination of matter disclosed in Nakamura, Muddu and Dansky.

Therefore, at the core of the dispute between the Examiner and the Applicant is that any combination of matter disclosed in Nakamura, Muddu and Dansky fails to teach or suggest all of the Applicant's claim limitations. "To establish a *prima facie* case of obviousness ... the prior art reference (or references when combined) must teach or suggest all the claim limitations." MPEP 2143 Therefore it is the duty of

the Examiner to show that all of the Applicant's claim limitations are "covered" by the cited prior art references. Upon review of the Examiner' pair of mailed Office Actions (a first mailed on April 9, 2003, a second mailed on September 8, 2003), it is evident that the Examiner has failed to provide a clear explanation of how the prior art references teach or suggest all of the Applicant's independent claim limitations.

Specifically, in the pair of Office Actions mailed on April 9, 2003 and September 8, 2003, the Examiner rejected each of independent claims 1, 18, 28, 29, 33, 50 and 60 by stating only that:

> . . . the Nakamura reference discloses, a machine readable storage medium with at least one processor (Figure 35, Item 6, Col. 7 Lines 39-50) and a string model (Figures 3, 5, 6, 9, 22A, 22B, 23, 24, 25, 26, 27, 28, 30A, 30B, 30C, 34).
>
> However the Nakamura reference does not explicitly disclose modeling a trace limped elements, cross capacitors, a pi model and applied noise voltage.
>
> The Muddu reference discloses modeling a trace (Figure 1), a pi model (Figures 8b, 8c).
>
> It would have been obvious, to one of ordinary skill in the art, at the time of the invention, to have modified the Nakamura reference with the Muddu reference because (motiviation to combine) when designing with sub-micron design rules for integrated circuit design accurate models for interconnect delay of logic gates are required for functional modes that reflect the true functioning on the substrate before expensive fabrication is performed.
>
> The Nakamura reference does not expressly disclose lumped elements, cross capacitors and applied noise voltage.
>
> The Dannsky et al. [sic] reference discloses lumped elements (Col. 7 Lines 9-67, Col. 8 Lines 1-6) cross capacitors (Col. 7 Line 16), and applied noise voltage (Col. 1, Lines 15-18, Lines 63-67, Col. 2 Line 1-17).
>
> It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the Nakamura reference with the Dannsky et al. [sic] reference because (motivation to combine) it is important to calculate in an efficient manner the voltage noise characteristics of an integrated circuit design (Dannsky et al. [sic] Col. 1 Lines 55-67, Col. 2 Lines 1-33).

Scrutinizing the Examiner's "reasoned analysis" carefully, it is clear that the Examiner has only stated the following in the affirmative as the teachings of the prior art references:

1) "the Nakamura reference discloses . . . a string model . . .";

2) "[t]he Muddu reference discloses modeling a trace . . ., a pi model . . ."

3) "[t]he Dannsky et al. [sic] reference discloses lumped elements, cross capacitors . . . and applied noise voltage"

The Applicant respectfully submits that the Examiner has fallen short of the burden placed on the Examiner to show that all of the Applicant's claim elements are covered by the Nakamura, Muddu and Dansky references. The Examiner has only shown that a few key words can be found in the prior art; and, likewise, has failed to show that whole concepts communicated by the Applicant's independent claim language can be found in the prior art. As such, it appears that the Examiner has done nothing more that perform a key word search and cobble up an Office Action without any understanding of the Applicant's independent claims or the teachings of the prior art.

Because the Applicant believes that all of the Applicant's claim limitations are not found in the combination of Nakamura, Muddu and Dansky, and because the Examiner has the burden of showing that all the Applicant's claim elements are covered by the prior art, and because the Examiner has failed to clearly articulate exactly how the cited references cover the Applicant's claims, the Applicant respectfully requests the Examiner to do the following:

1) **provide a clear explanation** where the claim limitation "reducing a string to a pi model, the pi model having a pair of cross capacitors" can be found from the Nakamura, Muddu and Dansky references;

2) **provide a clear explanation** where the claim limitation "a pair of cross capacitors associated with a pi model, the pi model reduced from a string having more than a pair of cross capacitors" can be found from the Nakamura, Muddu and Dansky references;

3) **provide a clear explanation** where the claim limitation "a plurality of cross capacitors on a node, each of the cross capacitors corresponding to a different proximate trace" can be found from the Nakamura, Muddu and Dansky references.

In the Office Action response mailed September 8, 2003 the Examiner has criticized the Applicant's comments in the Applicant's Office Action response mailed June 16, 2003. The Applicant respectfully submits that the Examiner's comments are off-point in a number of regards as elaborated on in more detail immediately below.

Firstly, the Examiner contends that the Applicant attempted to argue that the Nakamura reference is a non analogous art (See, Office Action mailed 9/8/03, Page

3). The Applicant made no such statement. Consistent with the Applicant's assertion that the combination of Nakamura, Muddu and Dansky fails to cover all of the Applicant's independent claim elements, the Applicant's statement that Nakamura "is an irrelevant prior art reference" (See, Office Action response mailed 6/16/03, pg. 17) is directed to the fact that there exists nothing of significance taught by Nakamura that could be used to cover anything claimed by the Applicant. Specifically, each of the Applicant's independent claims incorporate appropriate limitations that reveal the string to be a lumped element model of a trace (i.e., regarding Claim 1: "said string having a collection of lumped elements including cross capacitors"; regarding Claim 18: "said string having a collection of lumped elements"; regarding Claim 28: "said string having a collection of lumped elements including cross capacitors"; regarding Claim 29: "a string having more than a pair of cross capacitors"; regarding Claim 33: "said string having a collection of lumped elements including cross capacitors"; regarding Claim 50: "said string having a collection of lumped elements"; regarding Claim 60: "a string having more than a pair of cross capacitors"). The Nakamura reference uses the term "string" to refer to the surface of a semiconductor element without consideration of passive elements such as resistances and capacitances. Therefore the term "string" of Nakamura fails to cover the term "string" found in the Applicant's claims.

The Examiner has chastised the Applicant for not explicitly claiming "features upon which the applicant relies (i.e., Capacitive Coupling)" (See, Office Action mailed 9/08/03, pg. 3). Here, the Examiner seems to have failed to realize that the

phraseology "capacitive coupling between interconnect lines" that appeared in the Applicant's arguments in the Office Action response mailed June 16, 2003 were invoking the term "cross capacitor"; or, has refused to interpret the term "cross capacitor" in a manner that is consistent with that discussed from page 2, line 12 to page 3, line 7 of the Applicant's specification (See, Office Action mailed 9/08/03, pg. 3 : "[a]lthough claims are interpreted in light of the specification, limitations from the specification are not read into the claims"). If it is the later, the Applicant asserts that the issue with respect to the term "cross capacitors" is an issue devoted more to claim interpretation than to the incorporation of limitations into the claims. As such, the Applicant respectfully asks: what interpretation of the term "cross capacitor" is the Examiner using that is: a) inconsistent with that discussed from page 2, line 12 to page 3, line 7 of the Applicant's specification so as to allow the Examiner to dismiss the Applicant's arguments regarding the teachings of Muddu; yet, b) sufficient for the Examiner to use Dansky as a prior art reference against the term "cross capacitors" as it appears in the Applicant's claims?

Lastly, the Examiner seemingly attempts to avoid the burden of having to find each and every claim element in the prior art (so as to avoid having to establish a prima facie case of obviousness) by stating that the Applicant's attack on the prior art references is improper because "one cannot show non nonobviousness by attacking references individually where the rejections are based on combinations of references". The Examiner cites *In re Keller* and *In re Merck & Co.* to support the Examiner's position. The Applicant respectfully submits that the Examiner's

reference to *In re Keller* and *In re Merck & Co.* is an attempt to perversely distort the holdings of these cases.

In both *In re Keller* and *In re Merck & Co.*, the PTO Examiner found separate prior art references whose individual teachings and suggestions, when combined, covered all of the Applicant's claim elements. Hence, the issue in both these cases was whether or not non obviousness existed even though the examiner was able to find a teaching or suggestion of each claim element in the prior art. Because each claim element was actually taught or suggested by the prior art, the rejections of In re Keller and In re Merck & Co. were "based on combinations of references". Better said, whether or not the prior art references actually covered their corresponding claim elements was not in dispute.

In contrast, the Examiner's position in the present application effectively ignores the limitation "based on combinations of references" (i.e., that all claim elements are covered is not in dispute) so as to effectively read "one cannot show non obviousness by attacking references individually where the rejection is based on 35 USC 103(a)". This is a preposterous statement of the law because it removes the burden on the Examiner to establish a prima facie case of obviousness by finding each and every claim element in the prior art. The Applicant is certainly free, as is the situation in the present application, to demonstrate non obviousness by "attacking" a reference because it does not teach or suggest that which the Examiner purports it to so teach or suggest. That is, when the dispute is whether or not one or more claim elements are actually covered by a prior art reference, the

portion of *In re Keller* and *In re Merck & Co.* that has been cited by the Examiner does not apply.

The Applicant has also amended claim 17 to overcome an objection raised by the Examiner.

For reasons stated above the Applicant respectfully submits that all claims are in allowable form and respectfully requests the allowance of same.

CONCLUSION

Believing all claims to be patentable, the Applicant respectfully requests the allowance of same.

Applicants respectfully submit the present application is in condition for allowance. If the Examiner believes a telephone conference would expedite or assist in the allowance of the present application, the Examiner is invited to call Robert O'Rourke at (408) 720-8300.

If any additional fee is required, please charge Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

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